Amendments to the Claims

In response to the above mentioned Advisor action dated 3-19-2003, this listing of claims replaces all prior versions and listing of claims in the application.

1. (Currently and previously AMENDED) A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of:

a) forming a word line structure and a capacitor plate structure on a substrate;

(1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor;

b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure;

c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

d) forming a mask pattern over said cell node region;

e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node region ;

f) removing the mask pattern;

g) forming a dielectric layer over said substrate; and

h) forming a bitline contact to said second bitline region to form a 1T Static Random Access Memory.

2. (ORIGINAL) The method of claim 1 wherein said second bit line region preferably has an impurity concentration greater than the cell node region by at least a factor of 10.

3. (ORIGINAL) The method of claim 1 wherein said substrate is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said substrate has an impurity concentration between 1E17 and 1E18 atoms/cc.

4. (ORIGINAL) The method of claim 1 wherein said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between 1E17 and 1E18 atoms/cc.

5. (ORIGINAL) The method of claim 1 wherein said second bitline region has a concentration between 1E20 and 1E21 atom/cc.

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6. (ORIGINAL) The method of claim 1 wherein said first bit line region has a p-type doping and has an impurity concentration between 1E18 and 1E 19 Atoms/cc, said second bit line region has a p-type doping and has a impurity concentration between 1E20 and 1E21 atoms/cc and said cell node region has a p-type doping and has an impurity concentration between 1E18 and 1E19 atom/cc.

7. (ORIGINAL) The method of claim 1 wherein said first bit line region has a p-type doping and has an impurity concentration between 1E18 and 1E 19 Atoms/cc, said second bit line region has a p-type doping and has a impurity concentration between 1E20 and 1E21 atoms/cc and said cell node region has a p-type doping and has an impurity concentration between 1E17 and 1E18 atom/cc.

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8. (Currently amended and Previously TWICE AMENDED) A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of :

a) forming a dielectric layer on a substrate;

forming a conductive layer on said dielectric layer;

patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;

(1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor; said capacitor dielectric is comprised of said dielectric layer;

(2) said substrate is p doped and has a n-well under said word line structure and said capacitor plate structure, said N-well is doped with a second conductivity type impurity; second conductivity type impurity is an n-type impurity; said n-well has an impurity concentration between 1E17 and 1E18 atoms/cc;

C3 cont.

b) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure; said cell node region and said first bit line region do not intersect;

(1) said first bit line region and said cell node region have a p-type doping and have an impurity concentration between 1E18 and 1E 19 atoms/cc,

c) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

d) forming a mask pattern over said cell node region;

e) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node region; said second bitline region has a concentration between 1E20 and 1E21 atom/cc;

f) removing the mask pattern;

C3 cont'd

g) forming a dielectric layer over said substrate; and

h) forming a bitline contact to said second bitline region to form a 1T Static Random Access Memory.

Previously canceled claims 9-14.

Previously canceled claim 15.

9 ~~16~~. **(Currently amended and Previously Added)** A method of fabrication of a 1T Static Random Access Memory (SRAM), comprising the steps of:

a) forming a dielectric layer on a substrate;

b) forming a conductive layer on said dielectric layer;

c) patterning said conductive layer and said dielectric layer to form a word line structure and a capacitor plate structure on a substrate;

(1) said capacitor plate structure comprised of a capacitor dielectric on said substrate and a conductive plate layer on said capacitor dielectric; said capacitor plate structure overlying a plate region of said substrate; said plate region and said conductive plate layer acting as plates of a capacitor; said capacitor dielectric is comprised of said dielectric layer;

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d) implanting ions of a first conductivity type into said substrate forming a cell node region in said substrate between said word line structure and said capacitor plate structure; and forming a first bit line region in said substrate adjacent to said word line structure, said cell node region and said first bit line region do not intersect;

e) forming spacers on the sidewalls of said word line structure and said capacitor plate structure;

f) forming a mask pattern over said cell node region;

g) implanting ions of a first conductivity type into said substrate to form a second bitline region; and not implanting ions into said cell node region;

h) removing the mask pattern;

i) forming a dielectric layer over said substrate; and

j) forming a bitline contact to said second bitline region to form a 1T Static Random Access Memory.

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